AMENDMENTS TO THE CLAIMS

This listing of Claims will replace all prior versions and listings of claims in the application:

LISTINGS OF CLAIMS

1 – 23 (Cancelled)

24. (new) A computer system comprising:

a central processor;

a system reset generator coupled to said central processor for asserting a reset signal;

a system controller coupled to said central processor and said system reset generator, wherein said system controller comprises an SDRAM memory controller and a non-volatile memory controller;

addressable non-volatile memory coupled to said system controller, said system reset generator and said central processor, wherein said non-volatile memory comprises a sequential boot logic section;

a data bus coupled between said system controller and said non-volatile memory;

an SDRAM control signal line coupled between said SDRAM memory controller and said non-volatile memory, said SDRAM control signal line for carrying SDRAM control signals;

a first control signal line coupled directly between said non-volatile memory controller and said non-volatile memory for transmitting a chip select signal from said non-volatile memory controller in response to said reset signal, wherein said chip select signal is for initiating

a first read operation of a first data word at a first address in a first accessed row of said non-volatile memory; and

a second control signal line coupled directly between said non-volatile memory controller and said sequential boot logic section for transmitting a read enable signal to said non-volatile memory, wherein said read enable signal is for causing said non-volatile memory to deliver data words sequentially to said data bus beginning with said first data word, and wherein said sequentially delivered data words are for initializing an SDRAM interface of said non-volatile memory for normal operation with said computer system.

25. (new) The system of Claim 24 wherein said first control signal line and said second control line comprise a single control signal line.

26. (new) The system of Claim 24 wherein said first read operation is performed at a first address in a first accessed row of said sequential boot logic section of said non-volatile memory.

27. (new) The system of Claim 24 wherein said chip select signal is coupled to a pin on said non-volatile memory that does not receive SDRAM control signals.

28. (new) The system of Claim 24 wherein said chip select signal is coupled to a pin on said non-volatile memory that also receives SDRAM control signals.

29. (new) The system of Claim 24 wherein said sequential boot logic section comprises a storage area for data for configuring said SDRAM interface.

30. (new) The system of Claim 24 wherein said read enable signal and said chip select signal comprise an identical signal.

31. (new) The system of Claim 24 wherein said chip select signal issued in response to said reset signal always initiates a read operation to the same memory address regardless of any memory read address requested for reading by said central processor.

32. (new) The system of Claim 24 wherein parallel address lines are not connected between said non-volatile memory controller and said non-volatile memory.

33. (new) The system of Claim 24 wherein said non-volatile memory is a flash memory with an SDRAM interface.

34. (new) A method of configuring a non-volatile memory in a computer system, said method comprising:

issuing a system reset signal from a system reset generator upon booting of said computer system;

receiving an initial memory read address in a system controller, said initial memory read address supplied by said central processor;

issuing a chip select signal from a non-volatile memory controller of said system controller, wherein said chip select signal is issued to a non-volatile memory for initiating a first read operation of a first data word at a first address in a first accessed row of said non-volatile memory;

reading said first data word;

issuing a read enable signal from said non-volatile memory controller, wherein said read enable signal is issued to said non-volatile memory for causing said non-volatile memory to deliver data words sequentially to a data bus beginning with said first data word;

outputting sequential data words from said non-volatile memory beginning with said first data word, said sequential data words being output from a sequential boot logic section of said non-volatile memory; and

initializing an SDRAM interface of said non-volatile memory for normal operation with said computer system, wherein said initializing is performed in response to data from said sequentially output data words.

35. (new) The method of Claim 34 wherein said sequential boot logic section stores data for initializing said SDRAM interface.

36. (new) The method of Claim 34 wherein reading said first data word comprises reading said first data word from an identical memory address each time said system is booted, regardless of said initial memory address requested for reading by said central processor.

37. (new) The method of Claim 34 further comprising receiving said chip select signal at said non-volatile memory on a signal line coupled directly between said non-volatile memory controller and said non-volatile memory.

38. (new) The method of Claim 34 further comprising receiving said read enable signal at said non-volatile memory on a signal line coupled directly between said non-volatile memory controller and said non-volatile memory.

39. (new) The method of Claim 34 further comprising receiving said read enable signal and said chip select at said non-volatile memory on a single signal line coupled directly between said non-volatile memory controller and said non-volatile memory.

40. (new) The method of Claim 34 further comprising receiving said chip select signal at said non-volatile memory on a pin of said non-volatile memory that does not receive SDRAM control signals.

41. (new) The method of Claim 34 further comprising receiving said chip select signal at said non-volatile memory on a pin of said non-volatile memory that also receives SDRAM control signals.

42. (new) The method of Claim 34 wherein said chip select signal and said read enable signal comprise an identical signal.